

**Model Name: MSH61FP-FJ**

SHEET	TITLE
01	COVER SHEET
02	BLOCK DIAGRAM
03	POWER SEQUENCE
04	Processor HOST
05	Processor DDRIII
06	Processor PWR
07	Processor GND
08	DDRIII CHANNEL A & B
09	MINI PCIE ,Buzzer
10	DVI-I
11	PCH DMI, PCI, PCIE, USB
12	PCH HOST,LPC, SPI, PM, HDA
13	PCH HOST, SATA
14	PCH NVRAM, FDI, DISPLAY
15	PCH CLK BUFFER AND CLK GEN
16	PCH PWR,GND
17	SIO IT8772 &FRONT PANEL
18	FRONT & REAL USB
19	SWITCH POWER
20	LINNER POWER
21	VCC CORE & AXG
22	HDA CODEC ALC269&AUDIO JACK
23	RTL8111E-VL/RTL8105E-H
24	19V-IN DC to DC
25	BOM & PCB MODIFY HISTORY
26	
27	

**Revision 1.0**

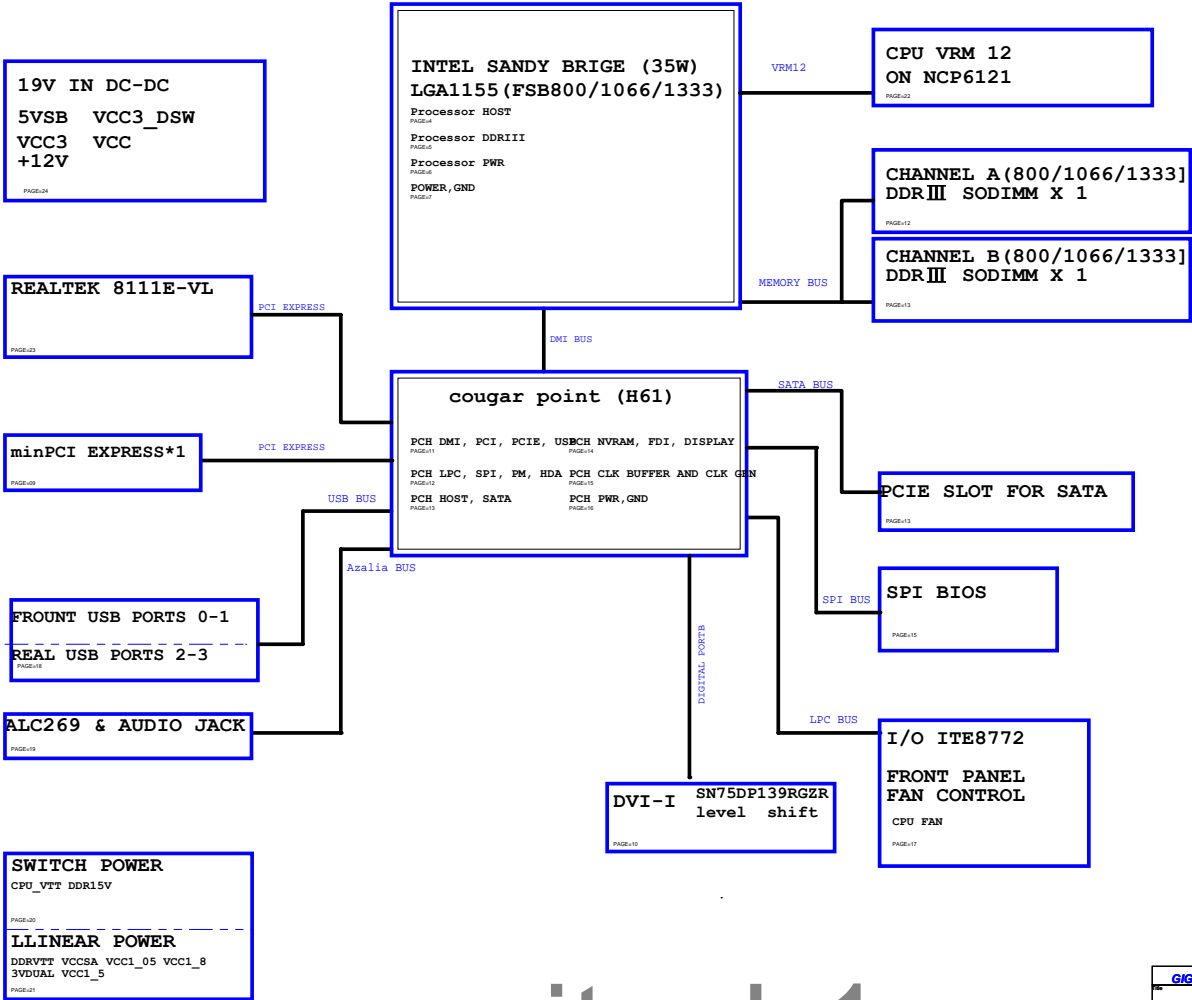
SHEET	TITLE
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GIGABYTE TECHNOLOGIES, INC.			
Cover Sheet			
Rev C	Document Number MSH61FP-FJ	Rev 1.0	
Date: Thursday, November 16, 2017 10:58 AM			

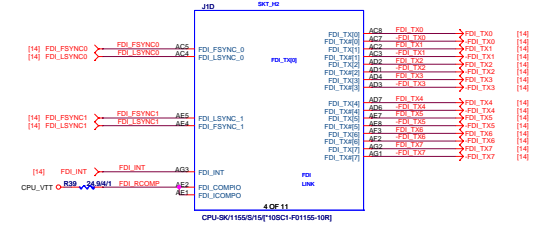
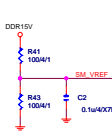
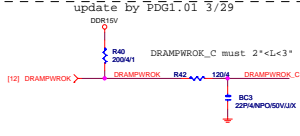
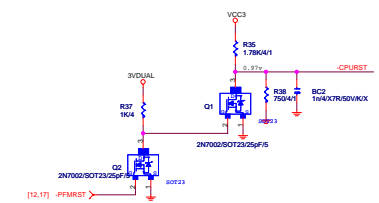
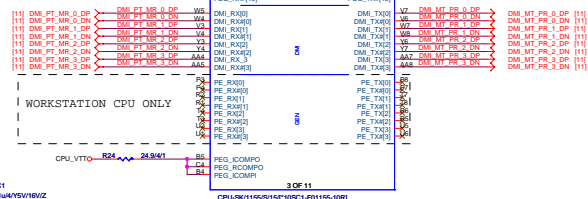
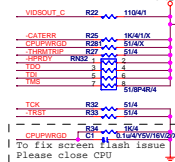
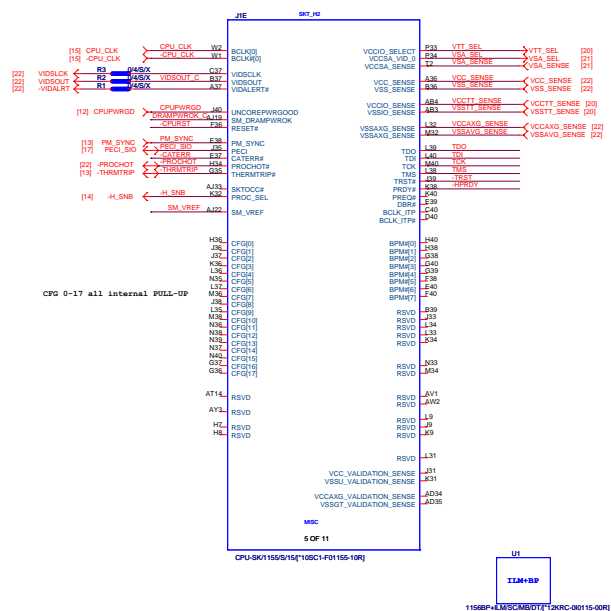
**TEKNISI INDONESIA**

BLOCK DIAGRAM

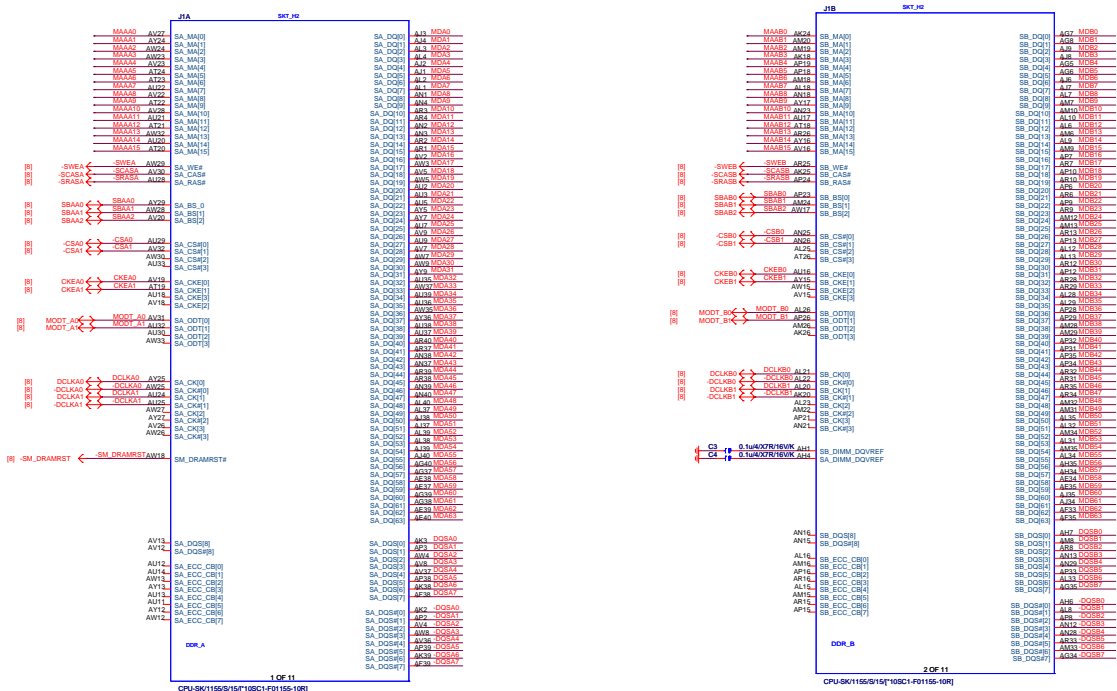


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GIGABYTE TECHNOLOGIES, INC.			
POWER SEQUENCE			
Doc	Document Number	MSH61FP-FJ	Rev
Control			1.0
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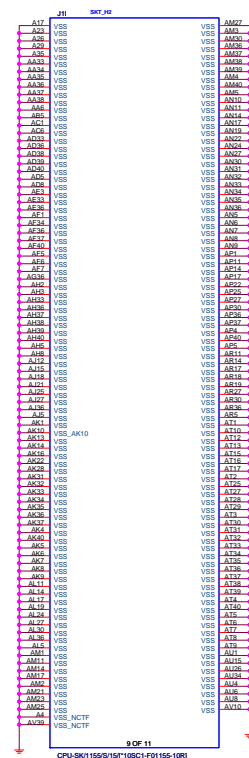
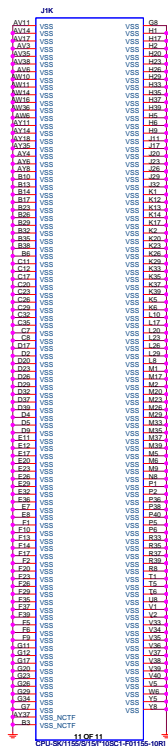
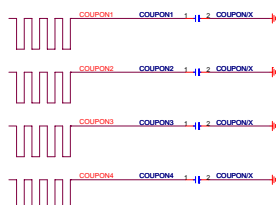
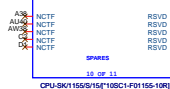


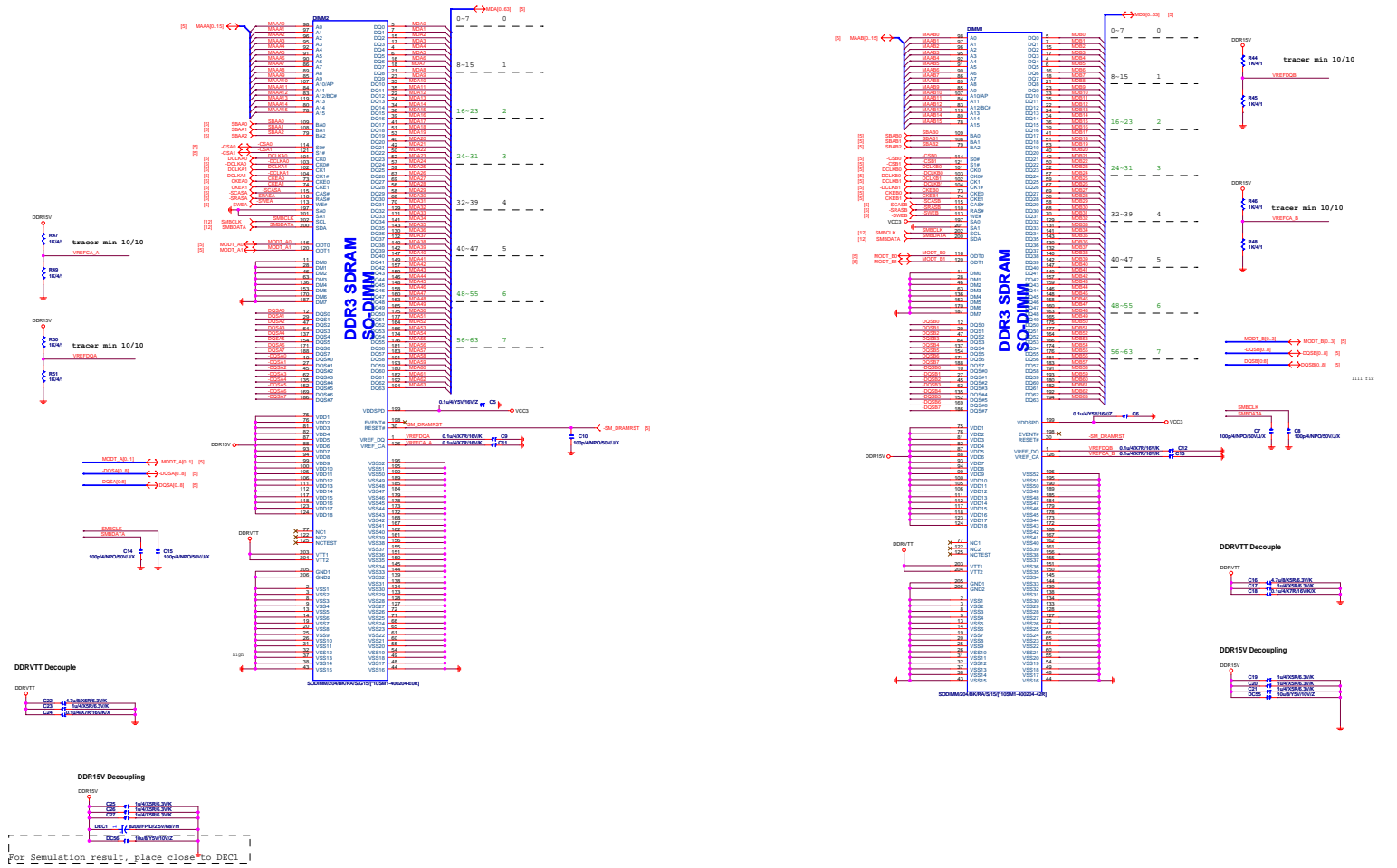
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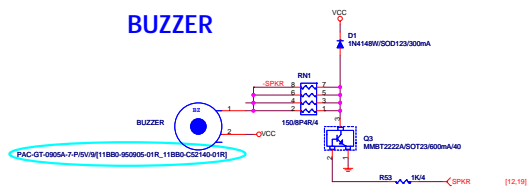




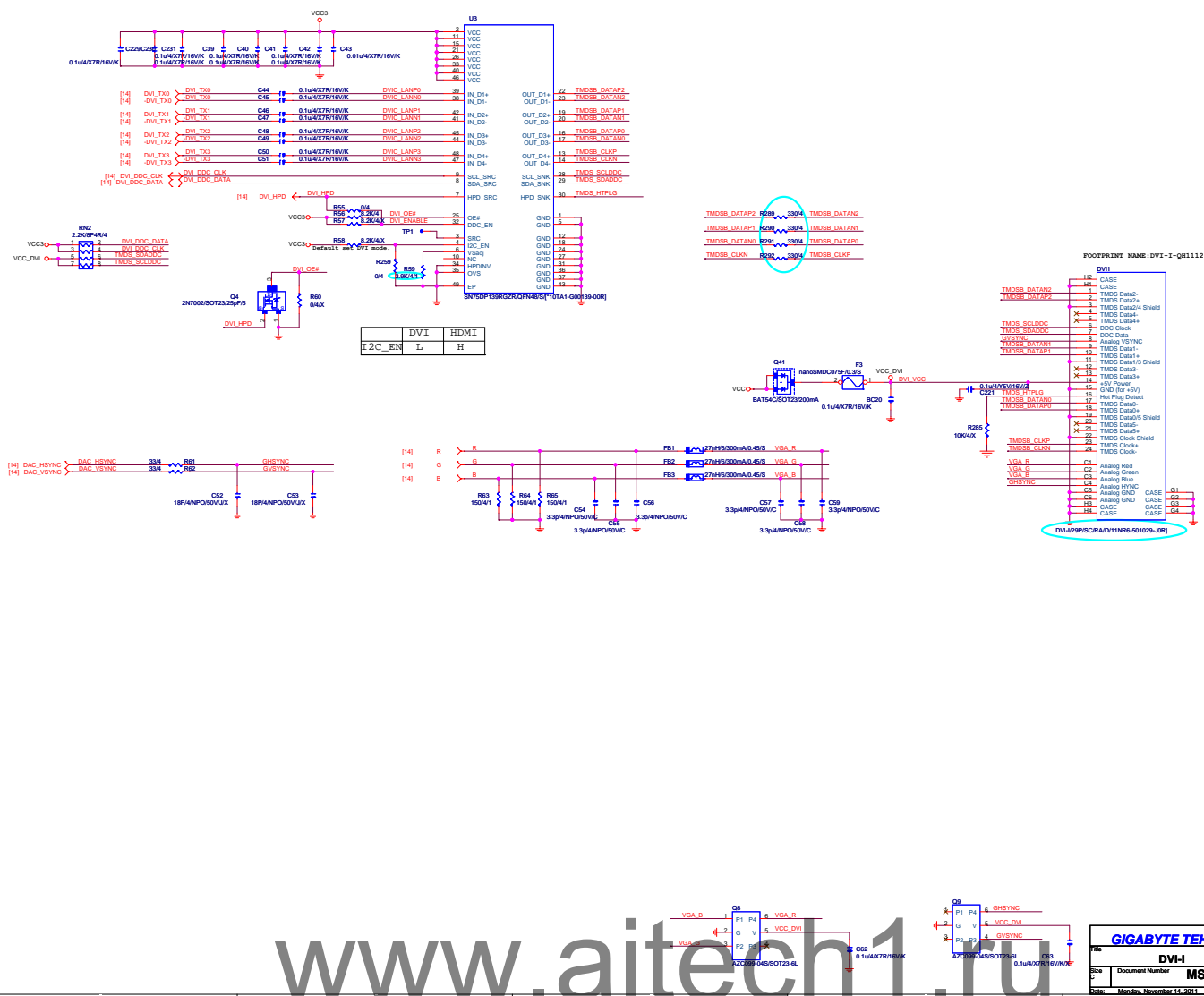


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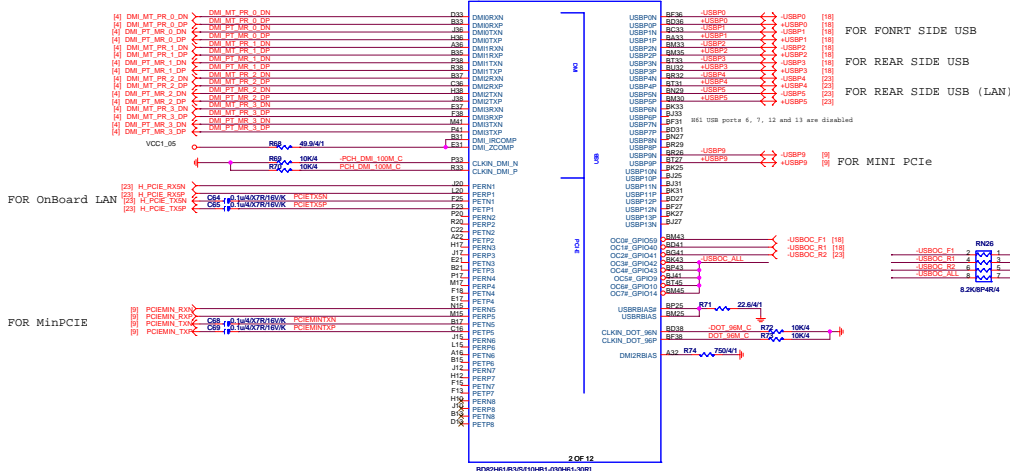
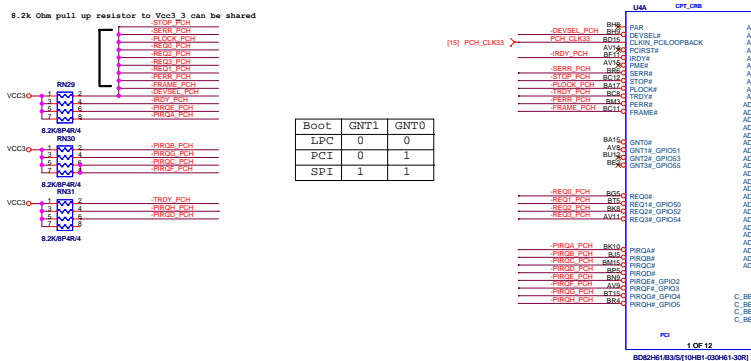


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Internal weak pull high  
and disable after PCIRST# de-assert

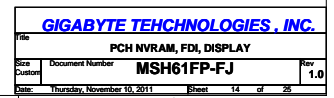
8.2k Ohm pull up resistor to Vcc3.3 can be shared



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Power On Strapping Options

Symbol	value	Description
JP4	K3PWR_EN	1 K3 power sequence function is disabled
Pin 126		0 K3 power sequence function is enabled
JP3 & JP5	FAN_CTL_SEL	11 The default value of EC Index 15h76h17h is 80h
Pin 124 & 46		10 The default value of EC Index 15h76h17h is FFh(Fan off)
JP2	WDT_EN	01 The default value of EC Index 15h76h17h is 00h(Fan full speed)
Pin122		00 The default value of EC Index 15h76h17h is 40h
		1 Disable WDT to rest PWROK
		0 Enable WDT to rest PWROK

If without use these pins, please pull-up. Don't let it floating

1.Pin 6: AT2955

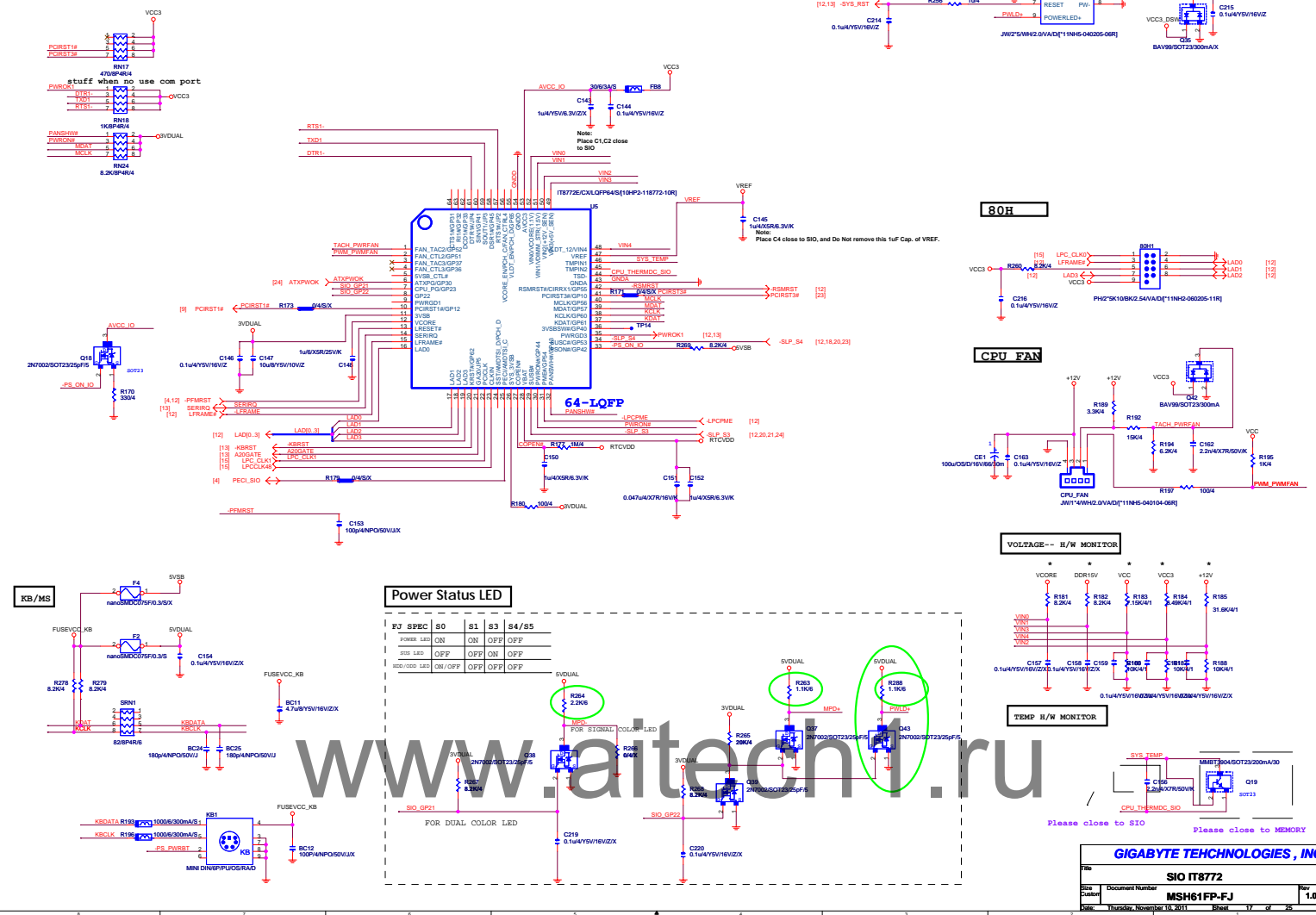
2.Pin 29: S0SB

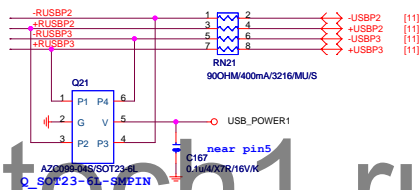
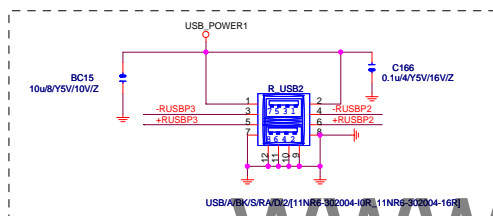
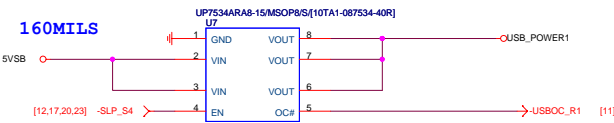
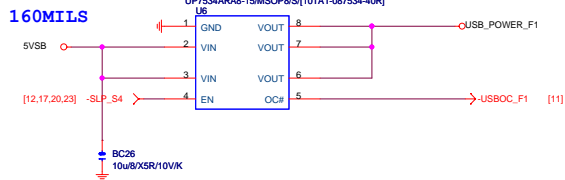
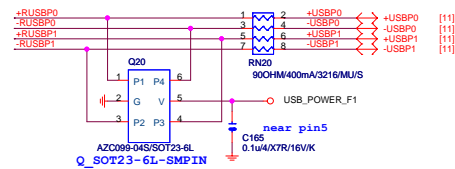
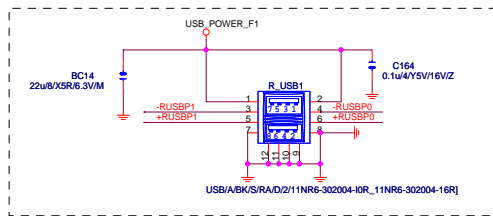
3.Pin 21/ Pin 57/ Pin 59/ Pin61

4.Pin37-40 KCLK/XDAT/MCLK/MDAT

5.Pin 63 pull high to 3VSB

Note: use Tuf function Pin29/ Pin30/ Pin31/ Pin34/ Pin47 pull high to 3VSB, Pin 5, Pin 32, pull high to 3.3VSB. Pin33 pull high to VCCN.

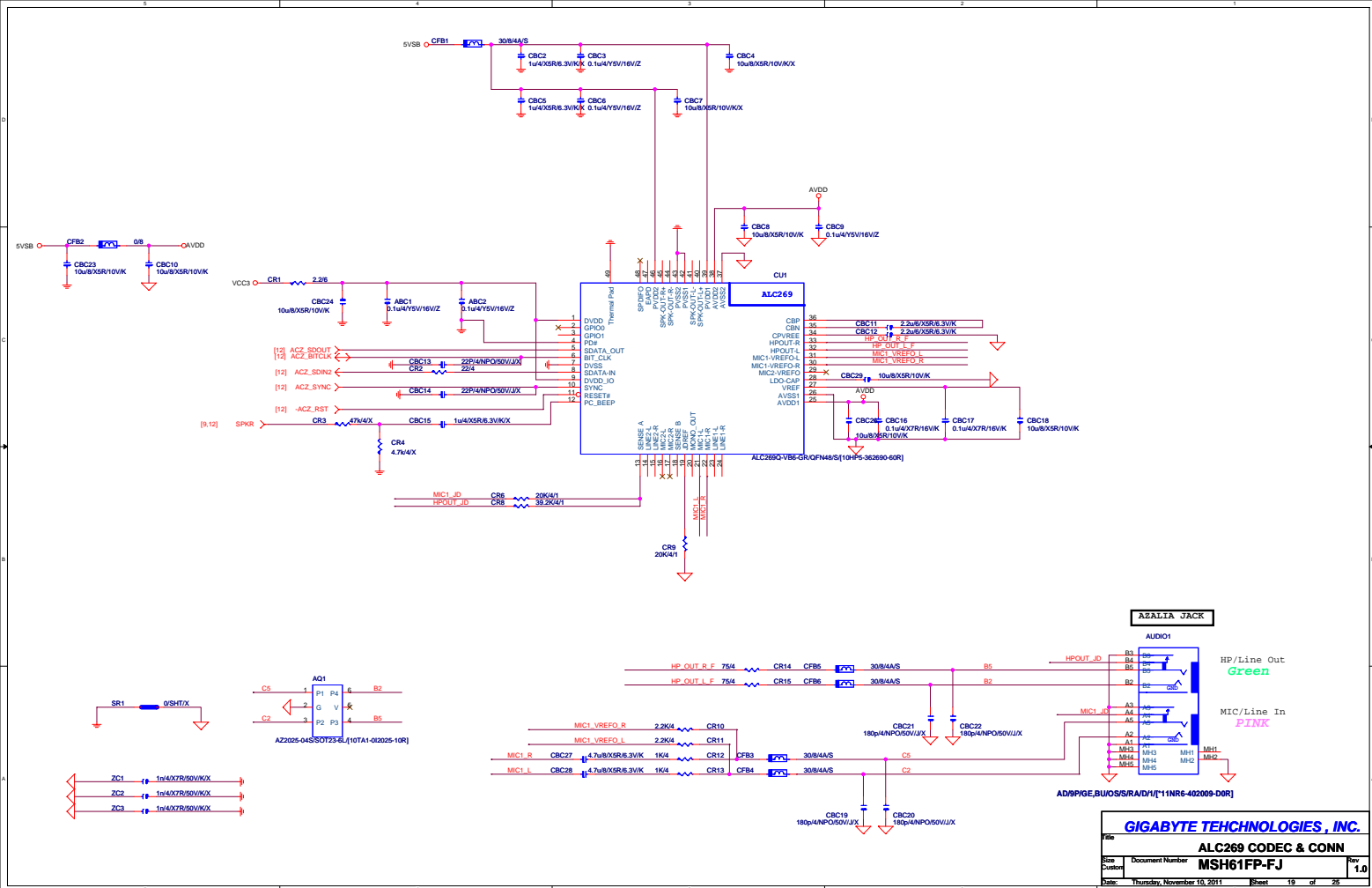




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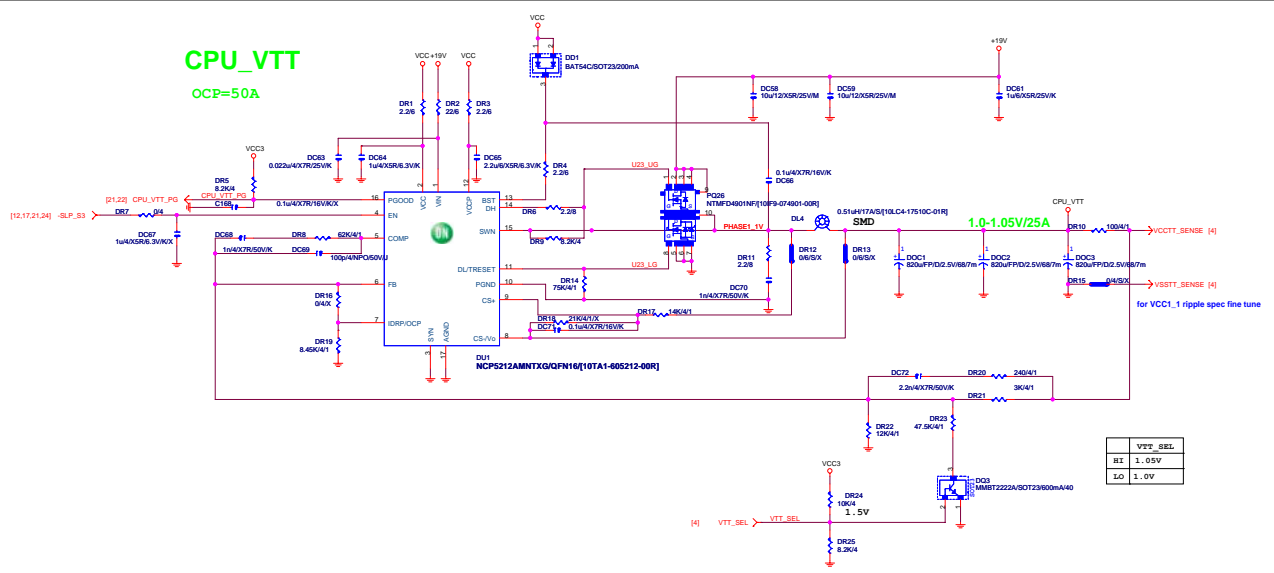
FRONT & REAL USB			
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Custom			1.0
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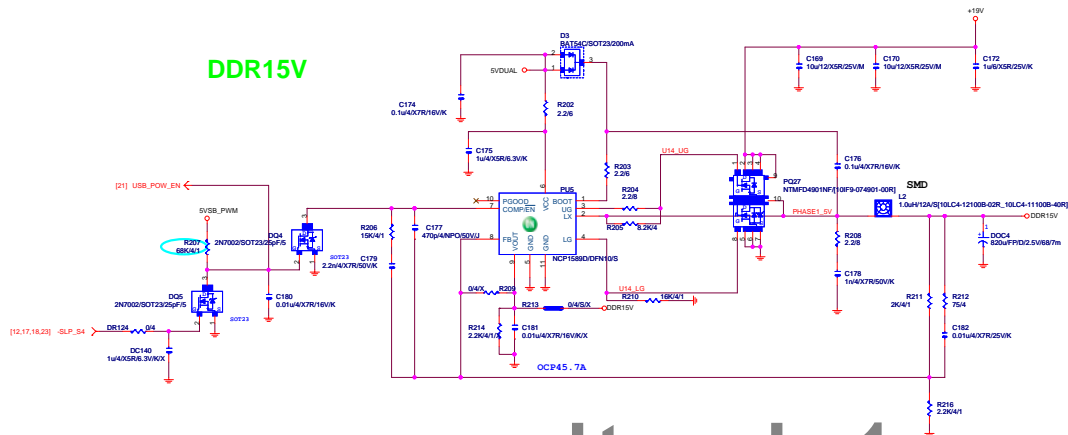
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## CPU\_VTT

OCP=50A

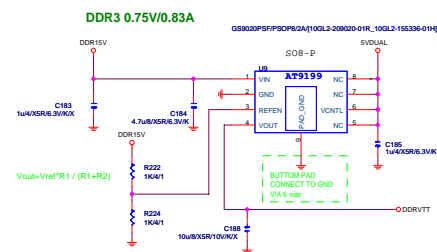


## DDR15V

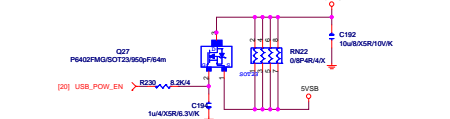


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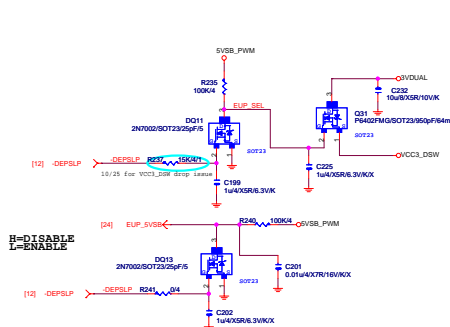
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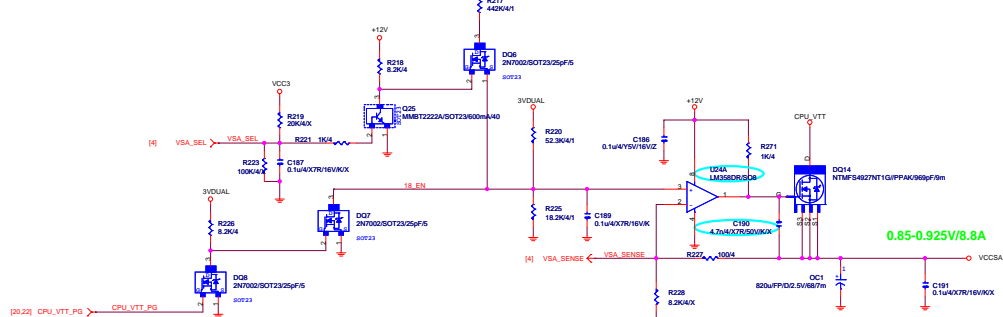
## 5VDUAL



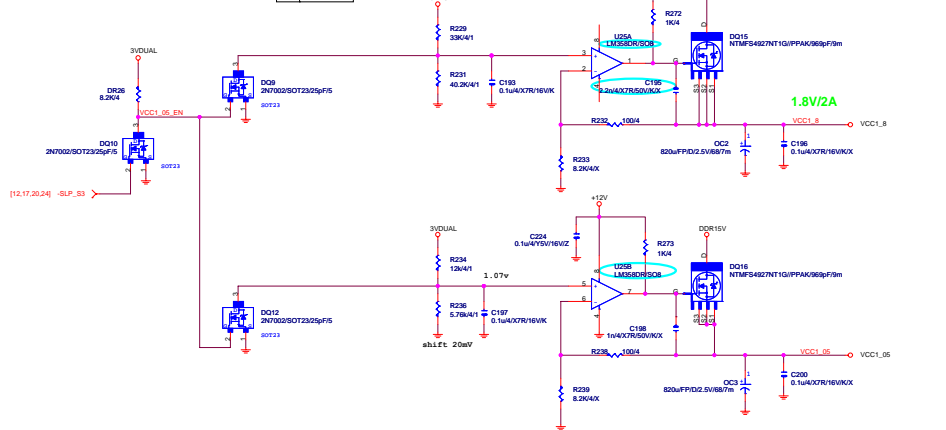
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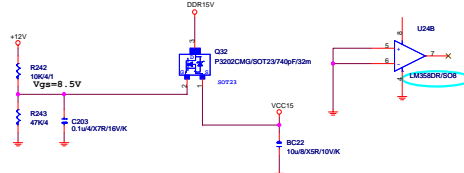
**VCCSA**



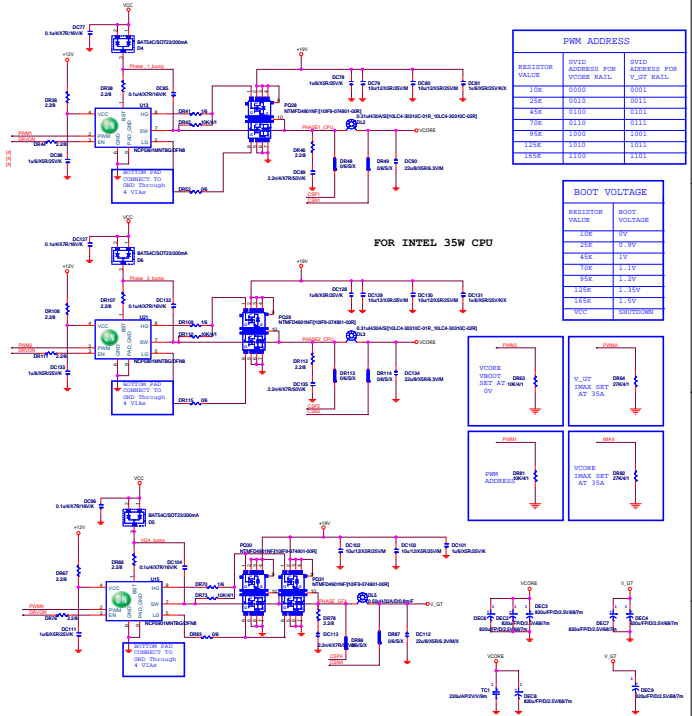
VCC18&VCC1\_05



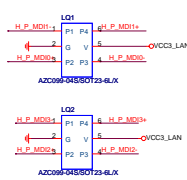
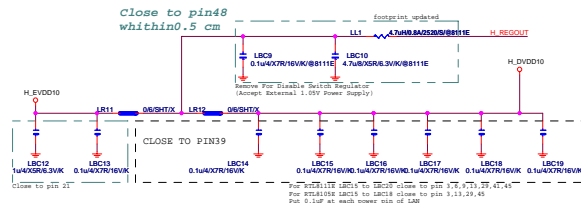
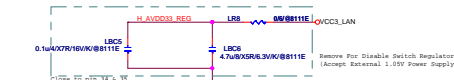
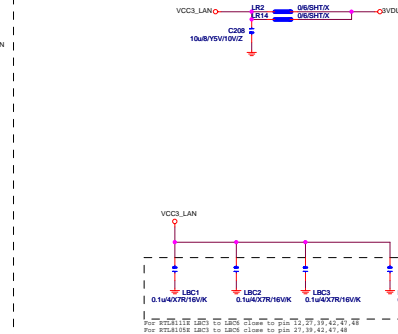
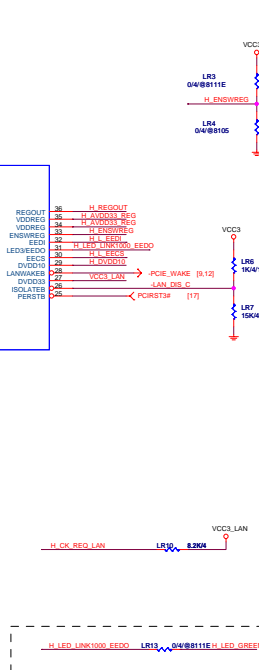
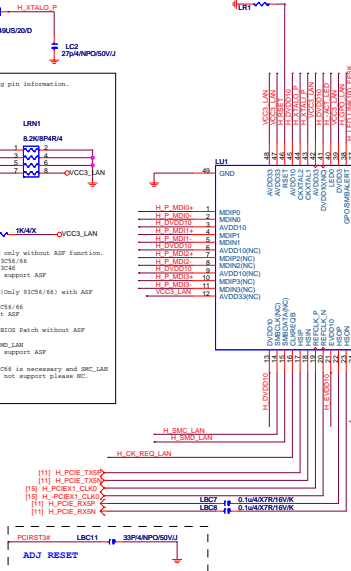
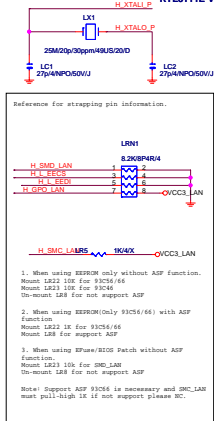
VCC15



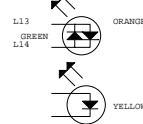
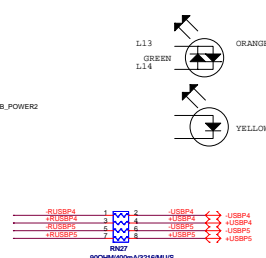
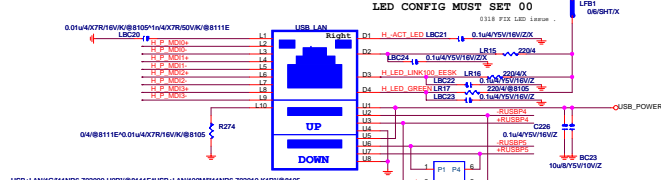
```
Vcore loadline=2.9 m ohm
Vaxg loadline=4.1 m ohm
```



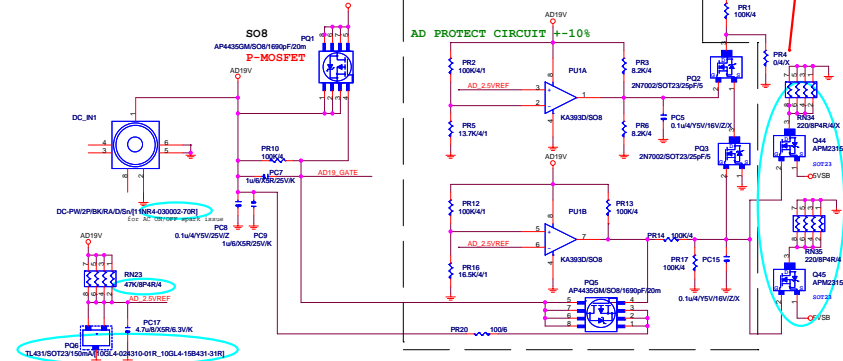
<b>GIGABYTE TECHNOLOGIES, INC.</b>			
<b>VCORE&amp;VGFX NCP6121</b>			
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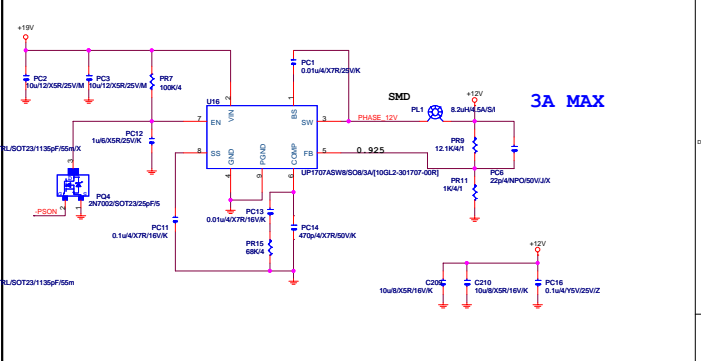
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1G		11NR6-702009-U0R



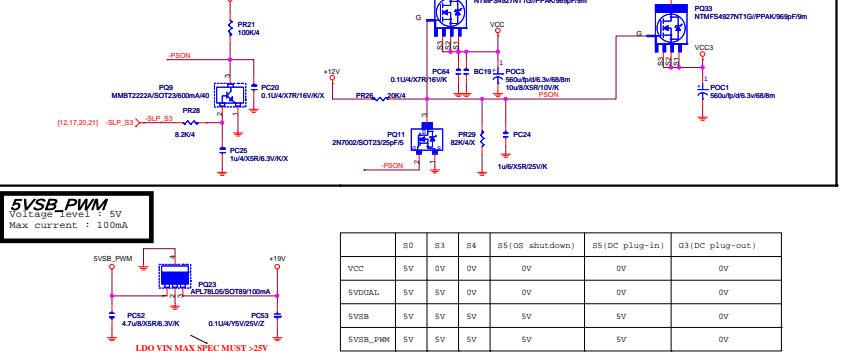
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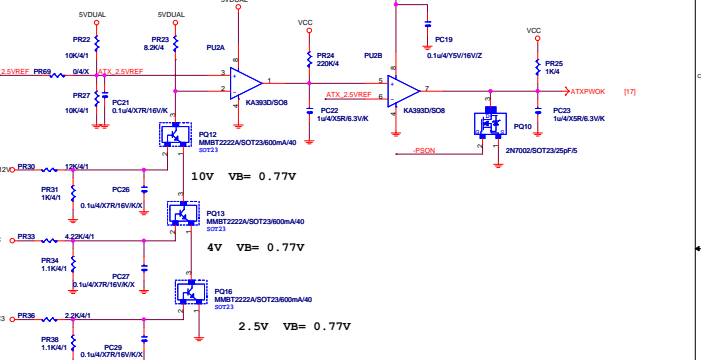
# +12V



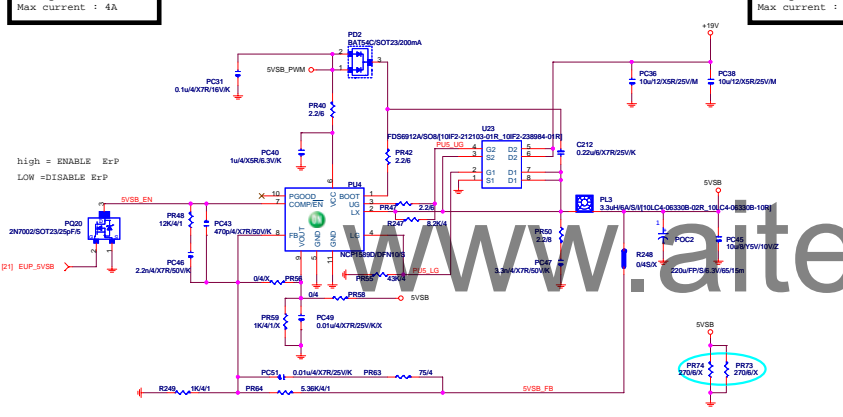
# VCC&VCC3



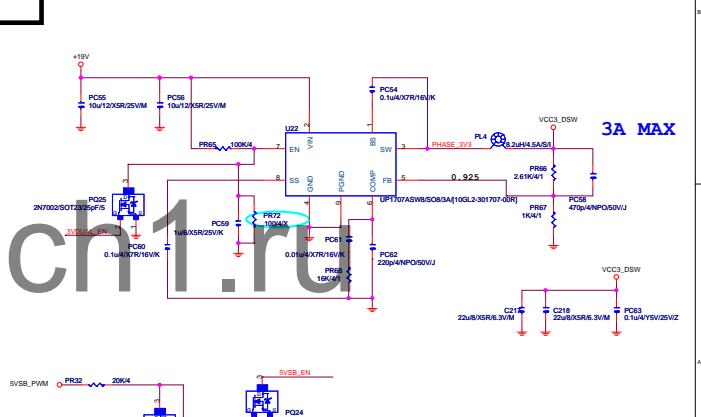
# ATX PPOWER GOOD



# 5VSB



# VCC3.DSW





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